In the Claims

Please cancel claims 2, 12-29, 34-40, and 45-51.

Please amend the claims as follows:

1. (Amended) A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and

[providing the divider circuit by placing a fixed-value divider at the input of the PLL to reduce the digital current created by the PLL.]

wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL.

5. (Amended) A method of reducing interference present in a circuit comprising the step of:

reducing [the] mutual inductance between digital circuitry in a first portion of the circuit and circuitry in a second portion of the circuit by placing a filter between the digital circuitry and a voltage source external to the circuit in order to reduce the area of a high frequency current loop.

41. (Amended) A method of reducing interference present in a circuit formed on an integrated circuit having PLL and VCO circuitry, the method comprising the step of:

[identifying circuitry in the circuit in which the impedance of the circuitry changes state over time during operation of the circuit; and]

[creating replica circuitry of the identified circuitry which operates in a state opposite of the identified circuitry.]

creating replica circuitry of first circuitry in the circuit which has an impedance that changes state during operation of the circuit, wherein the replica circuitry operates in an opposite state relative to the first circuitry.

42. (Amended) The method of claim 41, wherein the [replicated] replica circuitry has no function in the circuit other than reducing interference.

43. (Amended) The method of claim 41, wherein the [identified] first circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the [replica] second inverter is controlled to be in the opposite state of the [other] first inverter.

44. (Amended) The method of claim 41, wherein the replica circuitry is comprised of circuitry similar to the [identified] first circuitry, the method further comprising the step of connecting an inverter between an input of the [identified] first circuitry and an input of the replica circuitry.

Please insert the following new claims:

61. (New) A method of reducing interference present in a circuit formed on an integrated circuit, the method comprising the step of:

providing first circuitry in the circuit, wherein the first circuitry has an impedance that changes state during operation of the circuit; and

creating replica circuitry of the first circuitry, wherein the replica circuitry operates in an opposite state relative to the first circuitry.

62. (New) The method of claim 61, wherein the replica circuitry has no function in the circuit other than reducing interference.

63. (New) The method of claim 61, wherein the first circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the second inverter is controlled to be in the opposite state of the first inverter.

64. (New) The method of claim 61, wherein the replica circuitry is comprised of circuitry similar to the first circuitry, the method further comprising the step of connecting an inverter between an input of the first circuitry and an input of the replica circuitry.

65. (New) The method of claim 61, wherein the integrated circuit has PLL and VCO circuitry.

A copy of the pending claims (as amended) is attached.